CLAIMS

What is claimed is:

1.   A security access system for an integrated circuit
(IC), comprising:

an access code generator to generate a key code that
allows access to secured portions of the IC through a debug
module in the IC; and

a security portal arranged to receive the key code
from the access code generator, and allow access to the
debug module if the key code matches a pre-stored code in
the security portal.

2.   The system of claim 1, wherein said access code
generator includes a series of registers arranged to
provide the key code.

3.   The system of claim 2, wherein the key code is a
sequence of binary digits.

4. The system of claim 1, wherein said security portal includes

a key matching circuit to compare the key code entered by the access code generator with the pre-stored code in the security portal, where said key matching circuit generates an enable signal if the key code matches the pre-stored code.

5. The system of claim 4, wherein said key matching circuit includes a comparator.

6. The system of claim 4, further comprising:

a debug command enabling element arranged to allow access to the debug module when the enable signal is received from the key matching circuit.

7. The system of claim 6, wherein said debug command enabling element includes an AND gate.

8. The system of claim 6, further comprising:

a reset timer to provide a time window within which the key code from the access code generator is supplied to the key matching circuit, said reset timer de-asserting a key lock signal for a programmed time duration.

9. The system of claim 8, further comprising:

a key unlocking element arranged to pass the key code generated by the access code generator while the key lock signal is de-asserted.

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10. The system of claim 9, wherein said key unlocking element includes an AND gate.

11. The system of claim 8, wherein said reset timer includes at least one flip-flop.

12. The system of claim 8, wherein said reset timer includes at least one register.

13. An integrated circuit (IC) system, comprising:

a debugging tool;

a processor;

a plurality of peripheral devices coupled to said processor, said plurality of peripheral devices including secured portions, which may comprise secret codes or circuits;

a debug module coupled to said processor, said debug module arranged to receive commands from the debugging tool and to send data according to said commands;

an access code generator to generate a key code; and

a security portal disposed between said debug module and said debugging tool, said security portal allows the commands from the debugging tool to pass to the debug module only when the key code from the access code generator matches an internally stored code in the security portal,

such that said security portal operates to provide debugging tool with authorized access to said secured portions.

14. The system of claim 13, further comprising:

a bus connecting said plurality of peripheral devices and the processor, such that data communication is enabled among said plurality of devices and the processor.

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15.   The system of claim 13, wherein said plurality of peripheral devices includes memory devices having secret codes.

16.   The system of claim 13, wherein said processor is a central processing unit (CPU).

17.   The system of claim 13, wherein said processor is a digital signal processor (DSP).

18.   The system of claim 13, wherein security portal includes

a key matching circuit to compare the key code generated by the access code generator with the internally stored code in the security portal, where said key matching circuit generates an enable signal if the key code matches the internally stored code.

19.   The system of claim 18, further comprising:

a reset timer to provide a time window within which the key code from the access code generator is supplied to the key matching circuit, said reset timer de-asserting a key lock signal for a programmed time duration.

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20. The system of claim 19, further comprising:

a key unlocking element arranged to pass the key code generated by the access code generator while the key lock signal is de-asserted.

21. A method for accessing secured portions of an integrated circuit (IC) through a debug module, comprising:

receiving a key code;

determining if the received key code is correct; and

unlocking and enabling access to the debug module if a match is made.

22. The method of claim 21, wherein said determining includes matching the received key code with a pre-stored code.

23. The method of claim 21, wherein said unlocking and enabling includes passing a debug command to the debug module.

24. The method of claim 21, further comprising:

issuing a reset command to start a key unlock time window.

25. The method of claim 24, wherein said determining includes verifying that the received key code is correct, and that the key code is received within the key unlock time window.

26. The method of claim 21, further comprising:

locking and disabling access to the debug module if a match is not made.